Steady-State Dynamic Temperature Analysis and Reliability Optimization for Embedded Multiprocessor Systems

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I. Steady-State Dynamic Temperature Analysis

Introduction

Temperature is important.

Temperature Analysis

- Steady-State Temperature Analysis.
- Transient Temperature Analysis.
- Steady-State Dynamic Temperature Analysis.

Architecture Model

Multiprocessor systems running periodic applications.

$$\Pi = \{\pi_i = (V_i, \, f_i, \, N_{gate \, i})\}$$
 Core Number of gates Voltage Frequency

Power Model

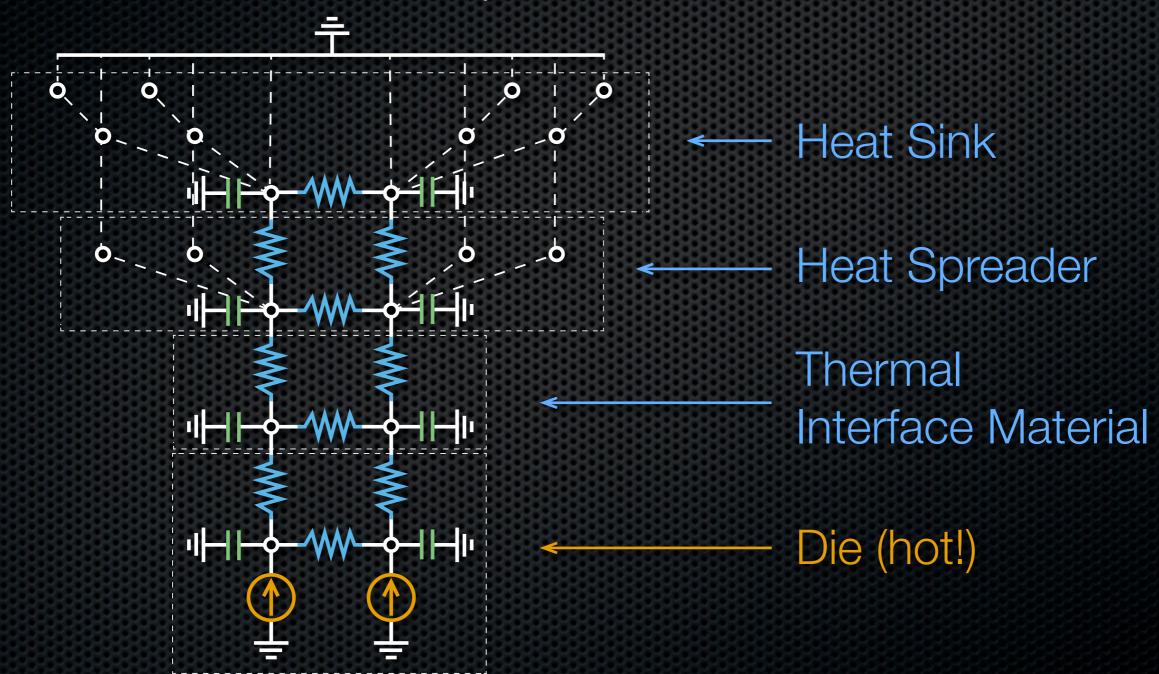
Total Power = Dynamic Power + Leakage Power

$$P_{dyn} = C_{eff} \cdot f \cdot V^2$$

$$P_{leak}(T) = N_{gate} \ V \ I_0 \left[A \ T^2 e^{rac{lpha \ V+eta}{T}} + B e^{(\gamma \ V+\delta)}
ight]$$
 Exponent Temperature

Thermal Model: RC Analogy

How to model temperature? Construct a circuit!



Thermal Model: Heat Equation

System of differential equations.

$$\mathbf{C} \frac{d\mathbf{T}(t)}{dt} + \mathbf{G} \left(\mathbf{T}(t) - \mathbf{T}_{amb} \right) = \mathbf{P}(t)$$
 Capacitance Temperature Conductance

Power & Temperature Profiles

Discrete dynamic power profile:

For all cores and all time intervals

$$\mathbb{P}_{dyn} \stackrel{\mathrm{def}}{=} \{P_{ij} : \forall i,j\}$$

Steady-State Dynamic Temperature Profile (SSDTP):

$$\mathbb{T} \stackrel{\mathrm{def}}{=} \{T_{ij} : \forall i, j\}$$

Problem Formulation

Given:

- Multiprocessor architecture.
- Periodic dynamic power profile.
- Floorplan of the die.
- Configuration of the thermal package.

Find:

Periodic temperature profile (SSDTP).

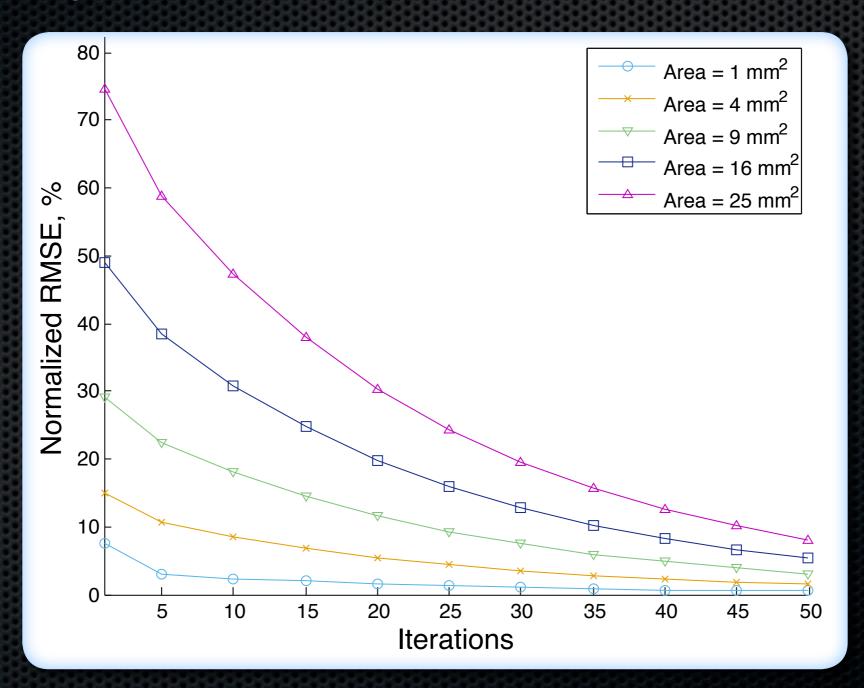






State of the Art Solutions: TTA

Looong transient temperature simulation.

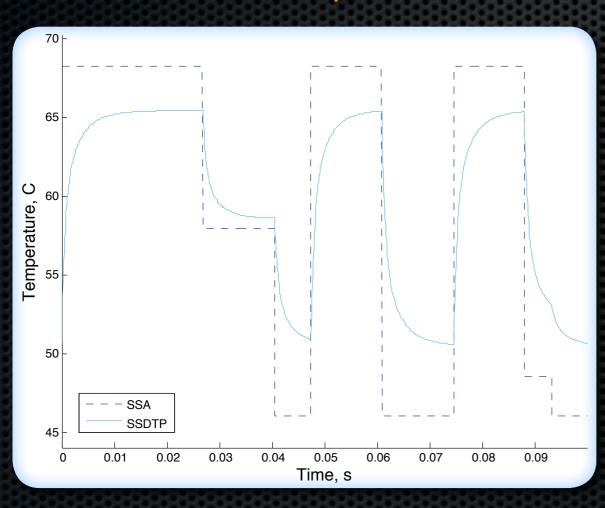


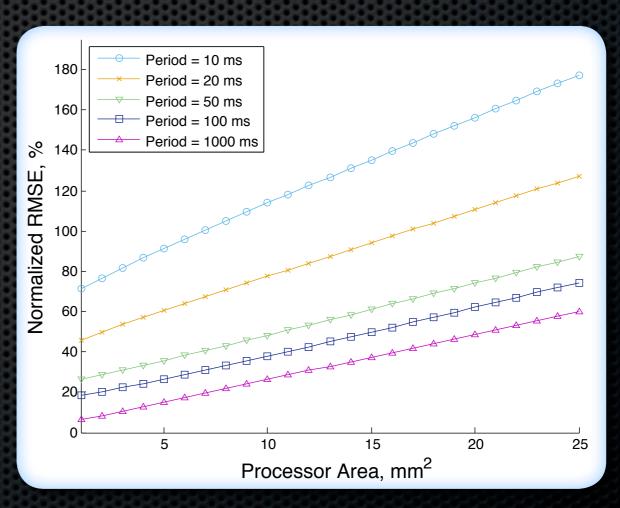


State of the Art Solutions: SSA

Approximation with steady-state temperature.



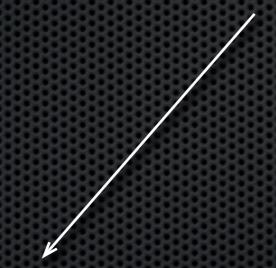




Analytical Solution

Heat equation can be solved analytically*.

$$\mathbf{T}(t) = e^{\mathbf{A}t} \mathbf{T}_0 + \mathbf{A}^{-1}(e^{\mathbf{A}t} - \mathbf{I}) \mathbf{C}^{-1}\mathbf{P}$$



Transient Temperature
Analysis

Steady-State Dynamic Temperature Analysis

Recurrence for SSDTP

Recurrent equation with a boundary condition.

$$\mathbf{T}_{i+1} = \mathbf{K}_i \, \mathbf{T}_i + \mathbf{B}_i \, \mathbf{P}_i$$
 $i=0,\dots,N_s-1$ $\mathbf{T}_0 = \mathbf{T}_{N_s}$ Number of steps

Linear System

System of linear equations.



Number of nodes

Number of steps

Straight-Forward Solutions

- Direct dense and sparse solvers.
- Iterative solutions.
- Block Toeplitz and circulant approaches (e.g., FFT).

Do not consider the structure.

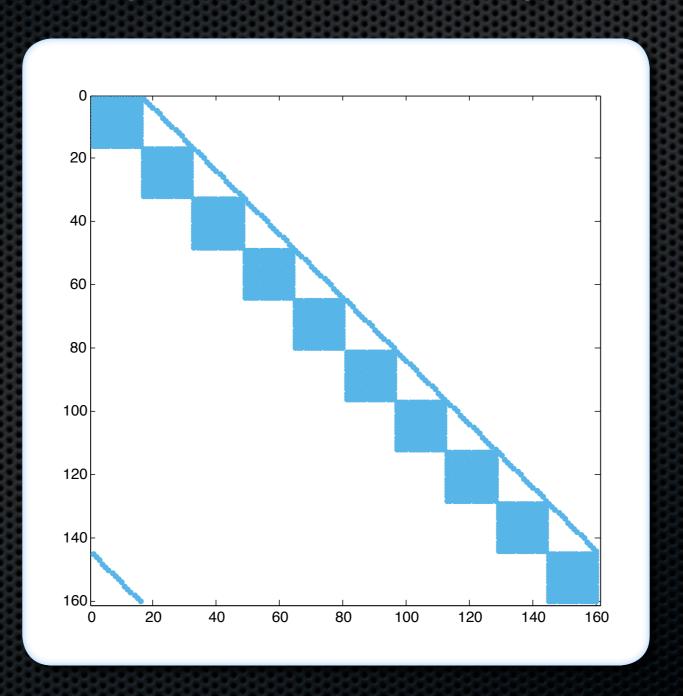
Do not consider the sparseness.



$$\propto N_s^3 N_n^3$$
 Memory consuming

Specific Structure

One block diagonal + two subdiagonals.



Proposed Method (PM)

$$\propto N_s \gg N_n$$

PM: Auxiliary Transformation

Expensive operations with matrices.

Exponent $\triangle A = A = A$

But not with symmetric matrices.

Eigenvalue decomposition

$$\mathbf{A} = \mathbf{U} \mathbf{A} \mathbf{U}^T$$

PM: Condensed Equation

Two successive recurrences.

$$egin{aligned} \mathbf{W}_0 &= \hat{\mathbf{Q}}_0 \ \mathbf{W}_i &= \hat{\mathbf{K}}_i \, \mathbf{W}_{i-1} + \mathbf{Q}_i, \ i = 1, \ldots, N_s - 1 \end{aligned}$$

$$\tilde{\mathbb{T}}_0 = \mathbb{U} (\mathbb{I} - e^{\tau \Lambda})^{-1} \mathbb{U}^T \mathbb{W}_{N_s - 1}$$
 $\tilde{\mathbb{T}}_{i+1} = \tilde{\mathbb{K}}_i \, \tilde{\mathbb{T}}_i + \mathbb{Q}_i, \ i = 0, \dots, N_s - 2$

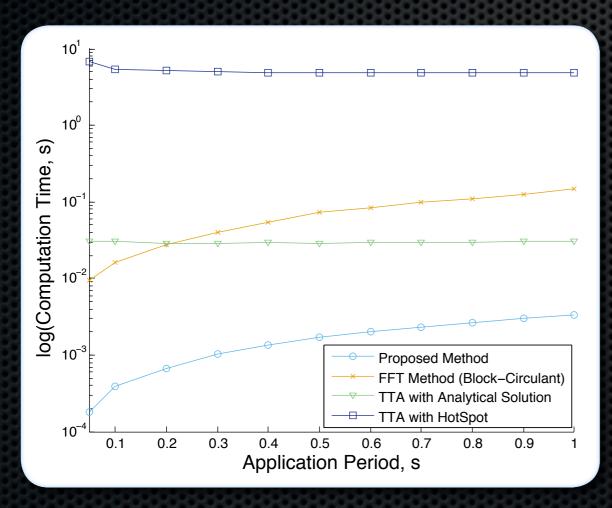
Features of the Proposed Method

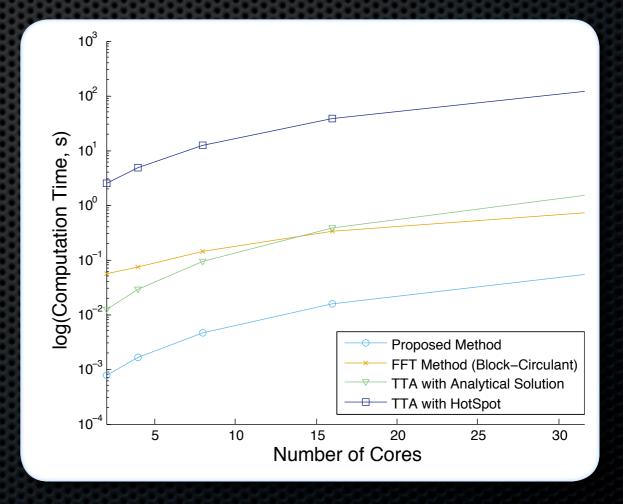
- Takes into account the structure.
- Coperates on a few small matrices.
- Linearly depends on the number of steps.
- **One-time** auxiliary work.

Performance

Scalability with period

Scalability with cores





II. Temperature-Aware Reliability Optimization

Application Model

Task graph of data-dependent tasks.

Application period
$$G=(V,\,E,\, au)$$

$$\begin{array}{ll} \text{Core} & \pi_j \in \Pi \\ \text{Task} & v_i \in V \end{array} \rightarrow (N_{clock} \ ij, C_{eff} \ ij) \end{array}$$

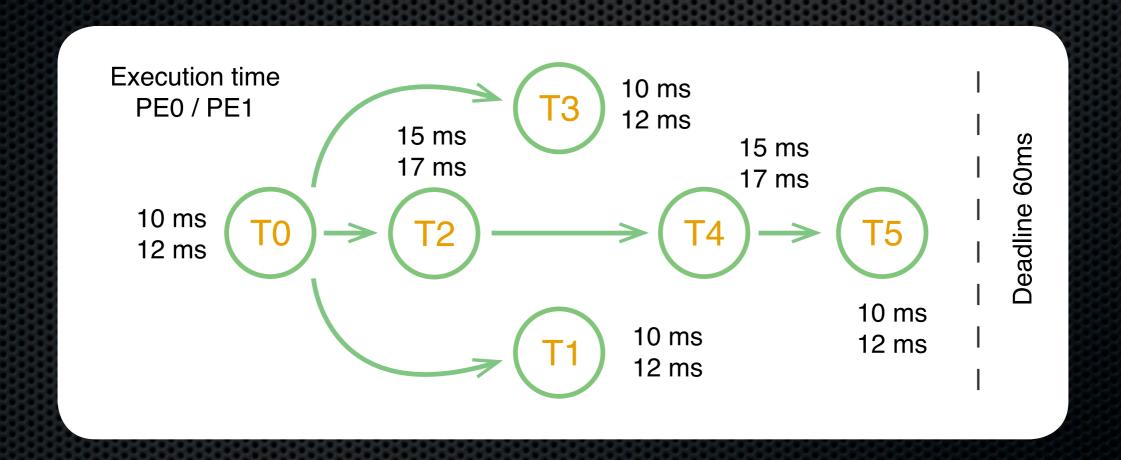
Reliability Model

Thermal cycling failure mechanism.

$$\mathcal{T} \sim Weibull(\eta, \beta)$$

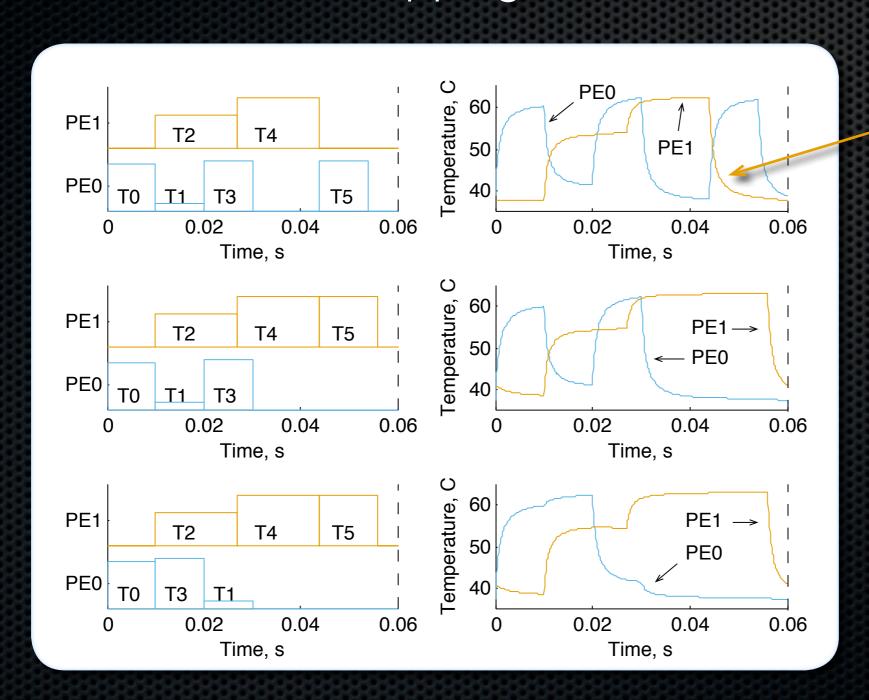
Motivational Example: Task Graph

Consider 2 cores and an application with 6 tasks...



Motivational Example: SSDTPs

Alternative mappings and schedules + their SSDTPs.



Thermal Cycling

+45% Lifetime

+55% Lifetime

Problem Formulation

Maximize:

Lifetime

$$\mathcal{F} = \min_{i=0}^{N_p-1} \theta_i$$

s.t.

$$t_{end i} \leq \tau \qquad \forall i$$
 $T_{ij} \leq T_{max} \qquad \forall i, j$

Genetic Algorithm

- Chromosomes encode mappings and priorities.
- Tournament selection.
- Uniform mutation.
- 2-point crossover.
- É Elitism model.

Experimental Results: Cores

- 20 tasks per core, 20 task graphs per each pair.
 - Lifetime improvement Computational time
- 4 cores & 80 tasks 39 times 34 seconds.
- ★ 8 cores & 160 tasks 28 times 4 minutes.
- 16 cores & 320 tasks − 8 times − 36 minutes.

Experimental Results: Tasks

- Quad-core chip, 20 task graphs per each pair.
 - Lifetime improvement Computational time
- 4 cores & 40 tasks 61 times 8 seconds.
- 4 cores & 80 tasks 36 times 32 seconds.
- 4 cores & 160 tasks − 29 times − 2 minutes.
- ⁴ 4 cores & 320 tasks 7 times 7 minutes.

Experimental Results: Techniques

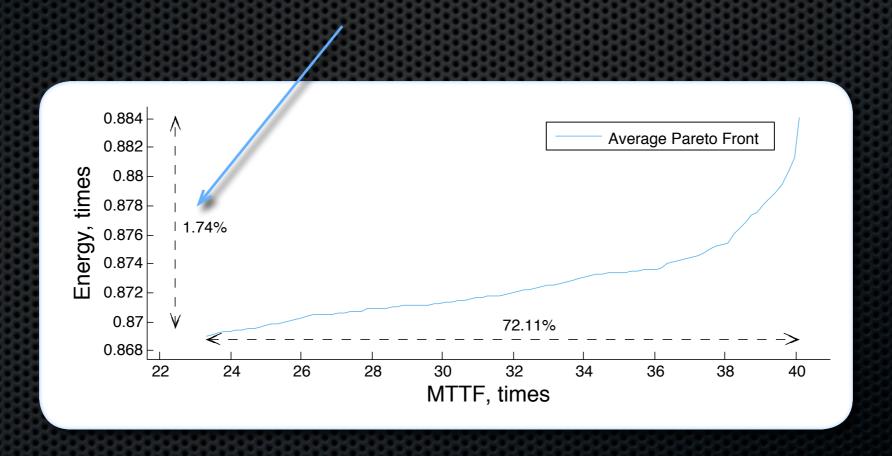
Comparison with the state of the art.

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We are here HotSpot SSA
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- 4/40 61 times 1 times 25 times.
- 4 / 80 36 times 2 times 14 times
- 4 / 160 29 times 2 times 5 times
- 4 / 320 7 times 2 times 4 times.
- **★** 4 / 640 4 times 1 times 2 times.

Experimental Results: Energy

Do not compromise the energy efficiency



Experimental Results: RLE

- Real-life example MPEG2 decoder.
- 2 cores.
- 34 tasks.

- 24 times longer lifetime with the proposed method.
- **5** times with HotSpot.
- **11 times** with the SSA.

Спасибо! Вопросы?

(не о девушках и кошках)